INTERNATIONAL SEARCH REPORT

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I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

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II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
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Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 3954465 (J.B. WELLS et al.) May 4, 1976, see column 2, lines 50-51; column 3, lines 50-51; column 4, lines 15-18	1,2,4
Y	EP, A1, 0023741 (PHILIPS) February 11, 1981, see page 2, line 32 - page 3, line 21; page 10, lines 18-27	1
Y	US, A, 4126528 (A. CHIANG) November 21, 1978, see column 1, line 34 - column 2, line 35	1,2,4
A		3
Y	L'Onde Electrique, volume 59, no. 10, October 1979 (Paris, FR) J.L. Ploix et al "Afficheurs par électrophorèse" see pages 65-69, in particular page 66, right-hand column	1
A	see paragraph III	4,6
A	Proceedings of the SID, volume 18, no. 3/4, 1977 (Los Angeles, US) I. Ota et al. ./.	

* Special categories of cited documents: [15]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [1]	Date of Mailing of this International Search Report [2]
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(71) Applicant: COPYTELE, INC. [US/US]; 900 Walt Whitman Road, Huntington Station, NY 11746 (US).

(72) Inventors: DISANTO, Frank, J. ; 27 Par Court, North Hills, NY 11030 (US). KRUSOS, Denis, A. ; 3 Middle Hollow Road, Lloyd Harbor, NY 11743 (US). SCHUBERT, Frederic, E. ; 18 Cordwood Path, Shoreham, NY 11786 (US).

(74) Agent: PLEVY, Arthur, L.; 146 Route 1 North, Edison, NJ 08817 (US).

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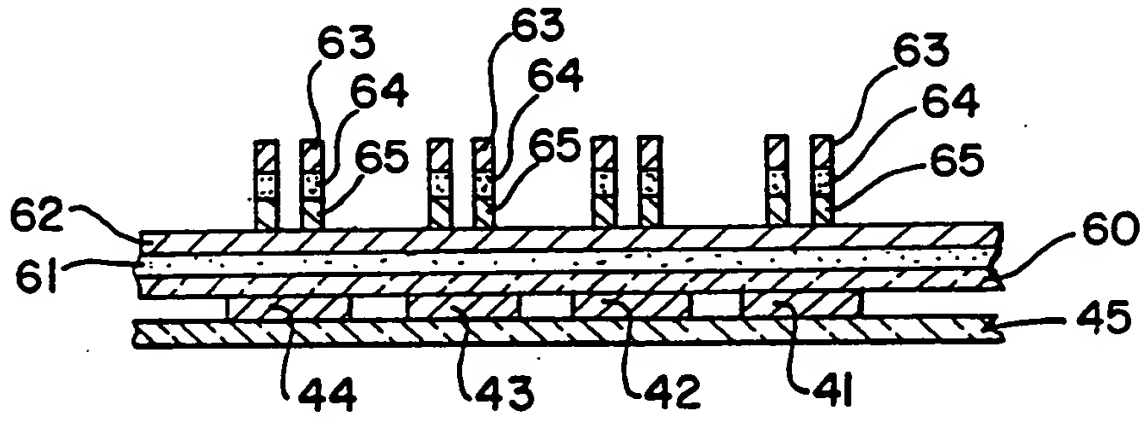
(54) Title: METHODS OF FABRICATING DUAL ANODE, FLAT PANEL ELECTROPHORETIC DISPLAYS



(57) Abstract

There is disclosed methods for fabricating electrophoretic displays (10). Essentially the methods employ selective materials such as different metals (15, 18, 19, 20) which are capable of being etched by different etchants. In this manner, a laminate is provided to form a grid matrix which is insulated from a cathode matrix (41, 42, 43, 44) which grid matrix is also insulated from a second anode matrix (54, 55). The entire display utilizes a local or second anode and a remote anode (28) to further control pigment particle migration. The display (10) is fabricated by two methods both of which employ selective etching of the parallel line type of display electrodes which constitute a cathode, a grid and a local anode.

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Description

Methods of Fabricating Dual Anode, Flat Panel Electrophoretic Displays

Technical Field

The present invention relates to electrophoretic display apparatus in general and more particularly to methods for fabricating such displays having a dual anode structure.

Background Art

A dual anode, flat panel, electrophoretic display apparatus has been described in copending application Serial No. 345,825 filed May 1, 1989 entitled Dual Anode Flat Panel Electrophoretic Display Apparatus for Frank J. DiSanto and Denis A. Krusos, the inventors herein and assigned to Copytele Inc., the assignee herein. That application describes an electrophoretic display which has a grid cathode matrix arrangement consisting of a first plurality of conductive lines which are transverse to said first plurality. Located with respect to the grid and cathode are first and second anode structures. The first anode is removed from the second with the second anode overlying the grid lines of the display and insulated therefrom. The second anode is biased to implement typical hold and erase modes independent of the first anode and the display structure as indicated in the application exhibits many advantages when compared with prior art displays.

The electrophoretic display (EPID) is well known and there exist many patents and articles in the prior art which describe operation and characteristics as well as describing methods of fabricating such displays. The following patents are illustrative of

prior art devices and approaches. These patents issued in the name of Frank J. DiSanto and Denis A. Krusos, the inventors herein. Apart from the patents to be described below, there are of course many references which were cited in the prosecution of these patents as well as additional references which were cited in the background of these patents. Many of the techniques and methods of fabricating such displays are disclosed in the patents that follow, as well as in the additional references as indicated.

U.S. Patent 4,655,897 issued on April 7, 1987 entitled Electrophoretic Display Panels and Associated Methods describes a typical electrophoretic display apparatus utilizing an X-Y matrix consisting of grid and cathode lines which are insulated one from the other and which are associated with an anode electrode. The space between the grid and cathode lines and the anode electrode is filled with an electrophoretic dispersion. The patent describes techniques for making such displays as well as suitable dispersions and materials for use with such displays.

U.S. Patent No. 4,732,830 issued on March 22, 1988 entitled Electrophoretic Display Panels and Associated Methods describes methods for making electrophoretic displays as well as describing display construction and operation.

U.S. Patent No. 4,742,345 issued on May 3, 1988 entitled Electrophoretic Display Panel Apparatus and Methods Therefore describes improved electrophoretic display panels exhibiting improved alignment and contrast as well as describing circuitry for use with such a display and methods for fabricating such a display.

U.S. Patent No. 4,746,917 issued on May 24, 1988 entitled Method and Apparatus for Operating Electrophoretic Displays Between a Display and a Non-Display Mode describes various biasing techniques for operating electrophoretic displays to provide writing, erasing as well as operating the display during a display and non-display mode.

U.S. Patent No. 4,722,820 issued on September 20, 1988 entitled Monolithic Flat Panel Display Apparatus describes methods and apparatus for fabricating flat panel displays employing electrophoretic principles as well structures to enable such displays to be biased and driven by additional circuitry.

Thus, as one can see, an important consideration of the prior art is to provide an improved display with increased contrast, faster operating time, and more reliable performance. As indicated in the above-noted copending application, a particularly disturbing problem which occurs in electrophoretic displays results in the appearance of a bright "flash" emanating from the display during the ERASE mode. This "flash" while occurring over a relatively short period is perfectly visible. The "flash" appears disturbing to many individuals who view the display and is caused by the following phenomenon. For proper operation of the electrophoretic display, the amount of pigment in the suspension is considerably greater than the pigment required to give a suitable background when the panel is in a HOLD condition. The term HOLD is well known in the art, and the electrophoretic panel is placed in a HOLD condition prior to writing the display. In this manner the HOLD condition is achieved when the anode is at a high

positive voltage, the grid is at a low voltage, and the cathode is at a high voltage.

Typically, the anode would be at a voltage for example of 200 volts with the grid at a lower voltage as for example -12 volts with the cathode at a high voltage which would be +15 volts. With these voltages on the typical prior art electrophoretic display, the display is in the so-called HOLD condition. This HOLD condition is implemented prior to the WRITE mode during which mode new information is written into the display. The excess pigment during the HOLD condition is at the surface of the anode which is at the highest potential with respect to any other of the electrodes. To ERASE the display, the anode is made negative and all the pigment leaves the anode and is at the surface of the grid and cathode. During ERASE, the anode, for example, would be placed at -200 volts. Hence, during the ERASE mode, all the pigment leaves the anode and is now at the surface of the grid and cathode accordingly. The cathode side of the flat display during the ERASE mode is considerably brighter than it is during the HOLD causing a bright "flash" to appear on the display even when the ERASE time is extremely short.

The "flash" occurs between frames and may exist every 20 to 30 milliseconds caused by the change in brightness between the HOLD and the ERASE mode. It is, of course, desirable to eliminate this bright "flash" so that the display appears more uniform and stable.

Hence, the above-noted copending application describes the addition of a second anode which is interposed between the original anode of the electrophoretic display and the cathode-to-grid

matrix. The second anode aides in preventing this flash by allowing the pigment to be selectively controlled.

This present application describes methods for fabricating a dual anode display. The methods to be described shows a second anode or an additional anode which in one embodiment is designed to be parallel with the grid structure and in another embodiment is transverse or perpendicular to the grid structure. These methods include the selective deposition of different materials such as metals and insulators together with the use of selective etches in order to achieve the desired results.

Disclosure of the Invention

A method of completing fabrication of an electrophoretic display after a plurality of cathode conductor lines indicative of an X matrix have been formed on a planar glass sheet, comprising the steps of coating the cathode conductor lines with a first insulating layer of photoresist, coating the first insulating layer with a first layer of silicon dioxide, coating a first layer of metal on said layer of silicon dioxide, coating said first layer of metal with a second layer of photoresist, coating said second layer of photoresist with a second layer of silicon dioxide, coating said second layer of silicon dioxide with a second layer of metal capable of being etched by a different etchant than said first, coating said second layer of metal with a third layer of metal capable of being etched by a different etchant from said first and second layer of metal, coating said third layer of metal with a fourth layer of metal capable of being etched by a different etchant than

said first, second and third layers of metal, coating said fourth layer of metal with a third layer of photoresist, treating said fourth layer of photoresist to photolithographically form a matrix of lines transverse to said cathode conductor lines and thereafter selectively etching each layer of material until channels separate each of the lines of said matrix wherein there are first and metal structures insulated from each other and from the cathode structure, coating the treated structure with a layer of silicon dioxide, removing said layer of silicon dioxide as coating said fourth metal layer with said fourth metal layer.

Brief Description of the Drawings

Fig. 1 is a partial cross-sectional view showing an electrophoretic display useful in describing certain steps in the fabrication of such a display;

Fig. 2 is a cross-sectional view depicting an additional step in the fabrication of such a display;

Fig. 3 is a top plan view of an electrophoretic display fabricated according to a different method according to this invention; and

Fig. 4 is a cross-sectional view of the display of Fig. 3.

Best Mode for Carrying Out The Invention

Referring to FIG. 1, there is shown a cross-sectional view of an electrophoretic display 10 constructed according to the teachings of this invention. It is immediately noted that the cross-sectional view of the display of FIG. 1 includes structure resulting from certain of the processing steps which are not complete.

It is believed that the configuration shown in FIG. 1 is necessary in order to fully understand the invention. The unique part of this particular display is the configuration as well as the method of producing the second or additional anode. The additional anode appears between the cathode 12 and the remote anode which is a conventional anode designated by reference numeral 28 in FIG. 2.

As seen from FIG. 2, the remote anode 28 is deposited upon a layer of glass 29. The remote anode 28 for example may be an extremely thin layer of indium-tin-oxide (ITO) which is deposited upon the layer of glass 29.

As one will further understand, the electrophoretic display is described in many of the prior patents as indicated above, and has a viewing area which includes a bottom glass sheet 11. Disposed upon sheet 11 are a plurality of cathode lines 12. These cathode lines are directed in a horizontal or vertical direction and are parallel to one another to form a matrix or grid of lines. A cross matrix, which is perpendicular to the cathode lines, consists of a series of parallel metal grid lines 15. These metal grid lines exist in prior art electrophoretic displays. The grid lines are separated from the cathode by means of an insulator material. This may be a dual layer of insulator material. A first layer consists of an insulator 13 which for example is a photoresist material such as FSC-L or FSC-M which essentially are novalac resins or phenolic resins. These resins are available as photoresist materials from a company called Shipley Products.

As seen in FIG. 1 and as will be further explained, the layer of photoresist or insulator 13

has deposited on the surface thereof a layer of silicon dioxide (Sio_2) 14. The layer of silicon dioxide is deposited on the layer of photoresist and thereafter a layer of metal 15 which constitutes the grid electrode is deposited upon the layer of silicon dioxide. In the construction shown in FIG. 1 and as will be further explained, deposited on top of the grid layer 15 is an additional layer 16 of photoresist which has deposited thereon an additional layer 17 of silicon dioxide. On top of the layer of silicon dioxide is a first layer of metal 18, a second layer of metal 19 and a third layer of metal 20. It is important that metal layers 15, 18, 19 and 20 be fabricated from metal materials which are capable of being etched by different selective etchants.

For example, such metal materials may comprise gold, aluminum, titanium-tungsten alloy, zironium as well as chrome. In this particular instance, the grid electrode layer 15 may be fabricated from chrome while the metal layers 18 and 19 may be an alloy of chrome and aluminum which will etch for example, by means of a different etchant other than the chrome layer. The above description indicates the deposition of separate layers which is in fact the case. The structure shown in FIG. 1 results after the steps of selective etching have been implemented as will be explained.

As one will see, the second anode which will include metal layers 18 and 19, and the grid structure as 15 are perpendicular to the cathode lines 12 and essentially the grid electrode 15 is parallel to and in line with the second anode conductor lines. Before describing the exact process by which the structure of FIG. is fabricated, a few comments will be made concerning the operation of the same. As one can

understand, the grid lines 15 which are separated from the cathode lines by means of the photoresist layer 13, and the layer of silicon dioxide 14 are disposed transverse to the cathode lines 12 and spatially intersect each cathode line to provide an X-Y matrix arrangement whereby a typical pixel area is accessed by addressing a grid and cathode line thereby providing a desired potential at the intersection between the two lines. This potential causes the migration of electrophoretic particles which are suspended in the electrophoretic suspension 30 and which particles migrate from the grid and cathode structure to the anode 28 (FIG. 2). The anode 28 is a very thin layer of metal as ITO deposited on a planar glass member 29 according to prior art teachings.

Typically, the thickness of the insulated areas as 13 and 16 are approximately 3 microns with the layers of silicon dioxide as for example, layers 14 and 17 being about 2000 Angstroms. In the structure shown in FIG. 1 the local anode which will be further described is of the same configuration as the grid structure. A local anode metal conductor line which eventually comprises metals 18 and 19 for example is separated from the grid line 15 by the insulating layer 16 and the layer of silicon dioxide 17. Thus, there are as many anode lines as there are grid lines. Each segment of the anode can have the same exact configuration as the associated grid segment. It is understood that the grid line can comprise a tine configuration as known in the prior art and such a configuration may or may not be used for the local anode lines. Hence, the grid format may be two or more tines with the anode line being a single line or a duplicate tine configuration.

For example, U.S. Patent No. 4,742,345 describes a grid structure fabricated with respect to the cathode structure in a tine configuration. Thus, one can utilize such a configuration to form the grid structure and therefore the anode structure. The advantages of such arrangements have been fully described in U.S. Patent No. 4,742,345. In this manner, and as explained in the above-noted copending application, it is further seen that the local anode structure may consist of a plurality of parallel lines each of which is associated with a grid line, and with each of the parallel lines being dimensioned and congruent with each of the associated grid lines as 15. The biasing of the various electrodes as shown in FIG. 1 has also been explained in detail in the above-noted copending application. Thus, the biasing of each electrode in HOLD, ERASE and WRITE modes has been explained as well as the movement of the pigment and the advantages of the display.

The methods of fabricating a dual anode display to be described herein employ alternate approaches. The cross-sectional view depicted in FIG. 1 shows certain steps in the fabrication of the display. As indicated, numeral 11 references a planar glass sheet. The glass sheet or plate 11 acts to provide a port through which a viewer of the display may discern image information set forth therein. The glass plate 11 is preferably coated with an extremely thin layer of indium-tin-oxide (ITO) as available as described in many of the above-noted patents. The layer of ITO 12 is relatively thin approximately in the range of 300 Angstroms in thickness so that the glass plate 11 retains its relative transparent characteristics. The cathode lines 12 are etched from the ITO layer which

is overcoated on the glass plate 11. This may be achieved as will be readily appreciated by those of ordinary skill in the art through conventional photo-etching or engraving techniques. Hence, a physical mask bearing representations of the cathode conductors as well as associated contact pads is employed to form an image of the plurality of cathode conductors 12 on the glass plate 11 and thereafter portions of the ITO coating not corresponding to the image are removed. More particularly, the glass plate 11 bearing the ITO layer may be initially overcoated with a photoresistive layer of any conventional form and thereafter masked having a conductive pattern associated with the plurality of cathode lines 12 displaced on the photoresistive layer. The glass plate is then exposed to ultraviolet light through the mask and developed.

The pattern remains and eventually is transformed into a plurality of cathode lines. Hence, the cathode is conventionally fabricated by means of prior art techniques leaving the glass layer 11 having on the surface thereof a plurality of cathode lines or column lines 12. One can gain further information regarding the construction utilizing the mask and related procedures by reference to U.S. Patent No. 4,742,345.

After this step, the entire structure is coated with an insulating layer of FSC-L or FSC-M. The are photoresist materials as above indicated and are novalac or phenolic resins. The insulating layers 13 are spun onto the surface of the glass plate having the cathode structure 12. Contrary to FIG. 1, an entire layer or coating 13 as shown by the line 31 is deposited upon the surface of the glass plate 11 having the cathode pattern 12 impressed thereon. The

entire surface is thus covered. Next a thin layer of silicon dioxide 14 is placed on the entire surface of the insulative layer 13. Again, this is done as a single coat. The layer of silicon dioxide is extremely thin and may be, for example, of a magnitude of 2000 Angstroms with the layer of photoresist being about 3 to 5 microns. After depositing the layer of silicon dioxide 14, a first layer of metal 15 such as aluminum is then deposited upon the silicon dioxide layer. The aluminum can be deposited by many well known techniques such as vapor deposition and so on. After depositing the layer of aluminum, another layer 16 of FSC-L or FSC-M is deposited on the aluminum layer. This layer 16 then has deposited on the surface another layer of silicon dioxide. Then three different metals are deposited on the layer of silicon dioxide. There is first deposited a layer of metal 18 followed by a layer of metal 19, followed by a layer of metal 20. Each of these metals must not be capable of being etched using the same etchant, or capable of being etched by the same etchant as used for the metal deposited on the first layer of FSC-L or FSC-M as layer 15 which is the grid layer. In any event, selective etchants employed for different metals are well known in the art as well as the different metals which are capable of being etched by using different etches. After the last layer of metal 20 is deposited, a coating of photoresist 31 is then spun onto the uppermost layer 20. The photoresist layer 31 is shown as a full layer as compared to the column structures depicted for the remaining portions of the grid. It is understood that the lines which are directed through each of the aluminum layers indicate

that total laminate is formed prior to the etchant steps.

The photoresist layer 31 is then exposed to a mask which is essentially similar in design to the grid mask and consists of a plurality of parallel lines and is placed transverse to the cathode structures. Thus the mask is used to expose the top photoresist layer 31 in order to eventually provide the column areas as indicated by reference numerals 33, 34 and 35. The photoresist layer 31 is then developed whereby the uppermost layer of the metal 20 is etched using an appropriate etchant for that layer and thus forming a first portion of the channel 36. The next two layers of metal 18 and 19 are etched using appropriate etchants which selectively attack that layer thus forming the further channels 37 and 38. The layer of silicon dioxide 17 is plasma etched using the metal layers as 18, 19 and 20 as a mask, thus forming the next portion of the channel or depression 39. The insulating layer 16 is then plasma etched completely down to the first layer of metal 15 thus forming the next portion of the channel 40. Then the first layer of metal 15 is then etched using an appropriate etchant for that layer forming the next portion of the channel 41. The layer of silicon dioxide between the layer 15 and the insulating layer 13 between the first layer of metal 15 and the cathode 12 is plasma etched.

Referring to FIG. 2, after the above noted procedure, one now has the upstanding vertical columns as shown separated by channels. Next the entire structure in FIG. 1 coated with a layer of silicon dioxide which layer is applied to the entire structure. Then using an appropriate etchant, the

upper most layer of metal is removed thereby removing the silicon dioxide covering the metal layer 20 as well the metal layer while leaving the metal layer 19 exposed. The side surfaces as well as the spacing between the side surfaces are all covered with an extremely thin layer of silicon dioxide 40. Then utilizing appropriate insulating spacers the anode which includes glass plate 29 and the remote anode structure 28 is attached to the treated structure. At the same time leads are made available not only for the second anode which consists now of metal layers 18 and 19 but also for the original anode is ITO layer 28. Thus as on can understand, the cell is now ready for accepting driver chips which are cemented and bonded to the glass plate in the usual manner and as for example described in U.S. Patent 4,772,820 as indicated above.

It has been determined that by providing a layer of silicon dioxide on the peripheral walls of each of the additional grid and second anode structure, one achieves extreme reliable performance in regard to the device.

Referring to FIG. 3 there is shown a top plan view of a partial section of an electrophoretic display made according to a second implementation. The top plan view of FIG. 3 show the structure prior to a final coating of silicon dioxide. Essentially, as seen from FIG. 3, the cathode lines which are deposited as described above, are designated by references numerals 41, 42 and 43. Disposed on top of the cathode lines and insulate therefrom are separate grid tine structures as 50, 51 and 53. The three tine structures 50, 51 and 53 represent for example, a single grid line. Aligned parallel with the cathodes

are the second anode lines designated by reference numerals 54 and 55 as associated with the cathode line 44. As will be explained the grid lines as 50, 51 and 53 are fabricated from a different metal than the second anode lines 54 and 55 constitute two lines for each cathode but may be more than two. The grid lines constitute three lines as 50, 51 and 53. The implementation of the display as well as the fabrication of the display can be best described by referring both to FIG. 3 and FIG. 4. As seen in FIG. 4, the bottom layer 45 which consists of glass has deposited thereon the ITO cathode layers as 41, 42, 43 and 44. The cathode matrix is fabricated as described above and is formed from a single layer of ITO which covers the entire glass sheet which ITO is then suitably etched or engraved to produce individual parallel cathode lines as 41, 42, 43 and 44. Thus the construction of the cathode is implemented utilizing the usual mask and procedures as described above. The next thing that occurs is that a complete layer 60 of FSC-L or FSC-M is deposited on and coats the entire cathode structure. Then a layer of silicon dioxide 61 is vapor deposited on or oxidized on the insulating layer 60. The next step in the procedure is to then deposit a layer of metal such as chrome which is layer 62 and deposited on the silicon dioxide layer 61. This layer of metal 62 constitutes the grid structure. A layer of photoresist is then spun on the metal layer 62. This layer is not shown. In any event, the layer of photoresist is then exposed by the grid mask in the usual manner and hence, one produces the grid line pattern as for example, 50, 51 and 53 on the photoresist layer which is spun on the metal layer 62. The grid mask is used to expose the photoresist in the

usual manner. After developing the photoresist, the metal is etched using a suitable etchant. As indicated, the metal layer 62 is chrome and one would then employ a chrome etchant. The photoresist layer is now stripped off in an appropriate solvent. The layer of silicon dioxide 61 is now plasma etched with the etched metal 62 serving as a mask. This therefore develops the appropriate grid structure. Next an insulating layer of FSC-L or FSC-M is deposited on the patterned metal layer and designated by referenced numeral 65. The insulative layer 65 is now coated with a thin layer of silicon dioxide 4. Deposited on top of the layer of silicon dioxide 64 is a second metal layer 63 which may be of a different material than the first layer. This layer 63 consists of two metal layers with a first layer of metal closest to the silicon dioxide layer 64 being the same as the first layer of metal 62. Each layer is capable of being etched by a different etchant. A layer of photoresist is now spun on the uppermost metal layer and completely covers the same.

It is understood that while the layers 63, 64 and 65 are shown as upstanding columns, it is expressly understood that these are distinct layers. After a top layer of photoresist is spun on the uppermost metal layer, a mask including tines similar to but not necessarily the same as the grid is placed on a photoresist such that the pattern is parallel to the cathode as 41 and 42 and perpendicular to the grid as grid line 62. After developing the photoresist, both metal layers are etched using appropriate etchants. The silicon dioxide layer 64 is plasma etched using the metal layers as composite layer 63 as a mask. Both the first and second layers of FSC-L or Fsc-M are

plasma etched down to the cathode as seen in the top view. Using an appropriate solvent, any residue from the plasma etching is removed. Then a coating of silicon dioxide is applied to the entire structure. Again, using an appropriate etchant, the uppermost layer of metal is removed thereby removing the silicon dioxide covering the metal and leaving the second layer of metal exposed. Using appropriate insulator spacers the remote anode is attached to the structure making sure that a lead is made available for connecting to the anode. The second layer may be connected with all leads in parallel, with each lead individually driven or with leads being driven in groups. The cell is now ready for accepting driver chips cemented and bonded in the usual manner.

Claims

1. A method of completing fabrication of an electrophoretic display after a plurality of cathode conductor lines indicative of an X matrix have been formed on a planar glass sheet, comprising the steps of:

coating the cathode conductor lines with a first insulating layer of photoresist,

coating the first insulating layer with a first layer of silicon dioxide,

costing first layer of metal on said layer of silicon dioxide,

coating said first layer of metal with a second layer of photoresist,

coating said second layer of photoresist with a second layer of silicon dioxide,

coating said second layer of silicon dioxide with a second layer of metal capable of being etched by a different etchant than said first,

coating said second layer of metal with a third layer of metal capable of being etched by a different etchant from said first and second layer of metal,

coating said third layer of metal with a fourth layer of metal capable of being etched by a different etchant than said first, second and third layers of metal,

coating said fourth layer of metal with a third layer of photoresist,

treating said fourth layer of photoresist to photolithographically form a matrix of lines transverse to said cathode conductor lines and thereafter selectively etching each layer of material until channels separate each of the lines of said matrix wherein there are first and second metal

structures insulated from each other and from the cathode structure,

coating the treated structure with a layer of silicon dioxide,

removing said layer of silicon dioxide as coating said fourth metal layer with said fourth metal layer.

2. The method according to Claim 1 further including the step of placing an anode plate parallel to said anode, cathode and grid matrices.

3. The method according to Claim 1, wherein the step of coating with an insulating layer of photoresist is coating with a phenolic resin.

4. The method according to Claim 1, wherein said first metal is chrome.

5. The method according to Claim 1, wherein said second metal is aluminum.

6. The method according to Claim 1, wherein said third metal is an aluminum chrome alloy.

7. The method according to Claim 1, wherein said fourth metal is an alloy of titanium and tungsten.

8. The method according to Claim 1, wherein said layers of silicon dioxide are about 2000 Angstroms thick.

9. The method according to Claim 1, wherein said layer of photoresist are between 3 to 5 microns thick.

10. The method according to Claim 1, wherein selectively etching includes etching said layers of silicon dioxide and said layers of photoresist by plasma etching.

11. The method according to Claim 1, wherein the steps of coating with a photoresist insulating layer includes spinning said photoresist on said layer.

12. The method according to Claim 1, wherein the metal electrode structure indicative of the grid matrix comprises a plurality of grid lines with each line comprising at least two tine members.

13. The method according to Claim 1, wherein one metal structure has lines parallel to the cathode lines, while the other metal structure has lines transverse to the cathode lines.

14. A method for fabricating an electrophoretic display of the type having an X-Y matrix for grid and cathode operation, comprising the steps of:

depositing a first thin layer of a conductive metal on a carrier plate of glass,

etching said layer to form a line pattern indicative of an X cathode matrix,

depositing a first insulating layer of a photoresist resin on said X cathode matrix,

depositing a first layer of silicon dioxide on said first layer of photoresist resin,

depositing a second layer of a conductive metal on said layer of silicon dioxide,

depositing a second insulating layer of a photoresist resin on said second metal layer,

exposing said second layer of photoresist with a Y grid matrix mask,

developing said photoresist according to said Y grid mask,

etching said second layer of said conductive metal to form said Y grid matrix,

removing the remainder of said second layer of photoresist,

etching said layer of silicon dioxide with said etched second layer of conductive metal serving as a mask,

depositing a third layer of photoresist resin on said etched second layer,

depositing a second layer of silicon dioxide on said third layer of photoresist,

depositing a first anode metal layer on said layer of silicon dioxide,

depositing a second different anode metal layer on said first anode metal layer,

depositing a fourth layer of a photoresist resin on said second different metal layer,

treating said fourth layer of photoresist to photolithographically form an anode matrix of lines parallel to said Y grid matrix and perpendicular to said X cathode matrix,,

etching said first ans second anode layers,

covering said structure with a thin layer of silicon dioxide and etching away said second layer of anode metal leaving said first anode layer to provide

an additional matrix designated as an anode matrix for said display.

15. The method according to Claim 14 further including the steps of placing an anode plate parallel to said anode, cathode and grid matrices.

16. The method according to Claim 14, wherein said first thin layer of a conductive metal is indium-tin oxide (ITO).

17. The method according to Claim 14, wherein said second layer of metal is chrome.

18. The method according to Claim 14, wherein said first anode metal layer is aluminum with said second anode metal layer being chrome.

19. The method according to Claim 14, wherein the step of depositing a photoresist resin on said X cathode matrix is spinning said resin on said X cathode matrix.

20. The method according to Claim 14 wherein the steps of etching said layer of silicon dioxide is plasma etching said layer.

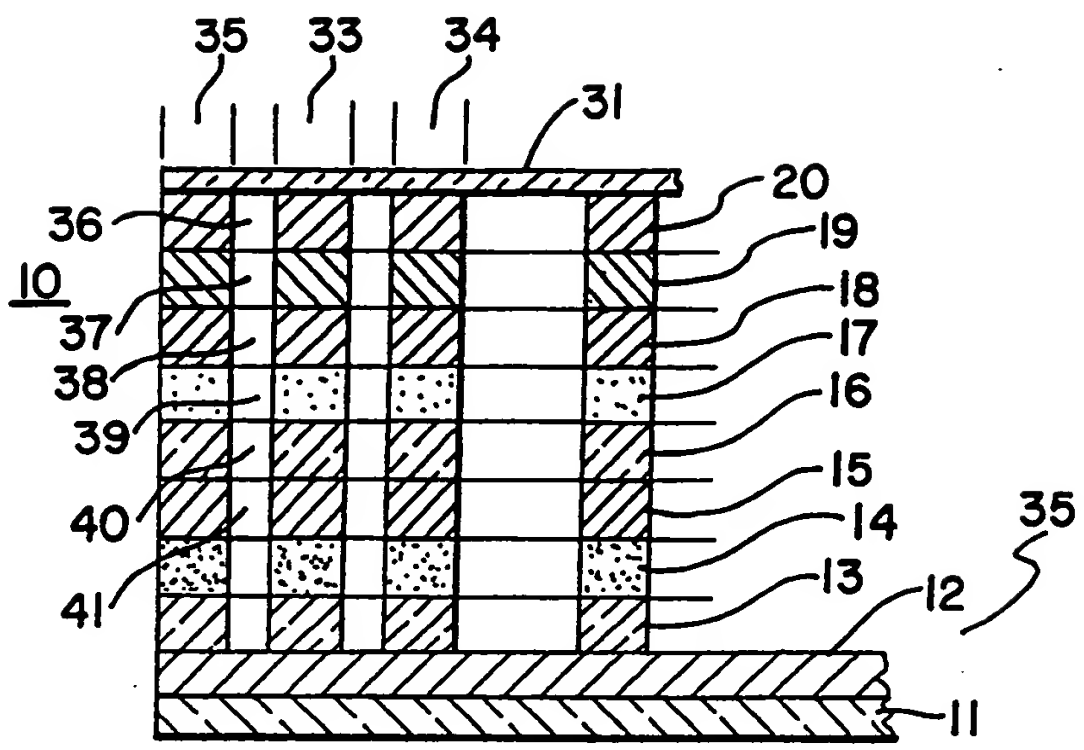
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FIG. 1

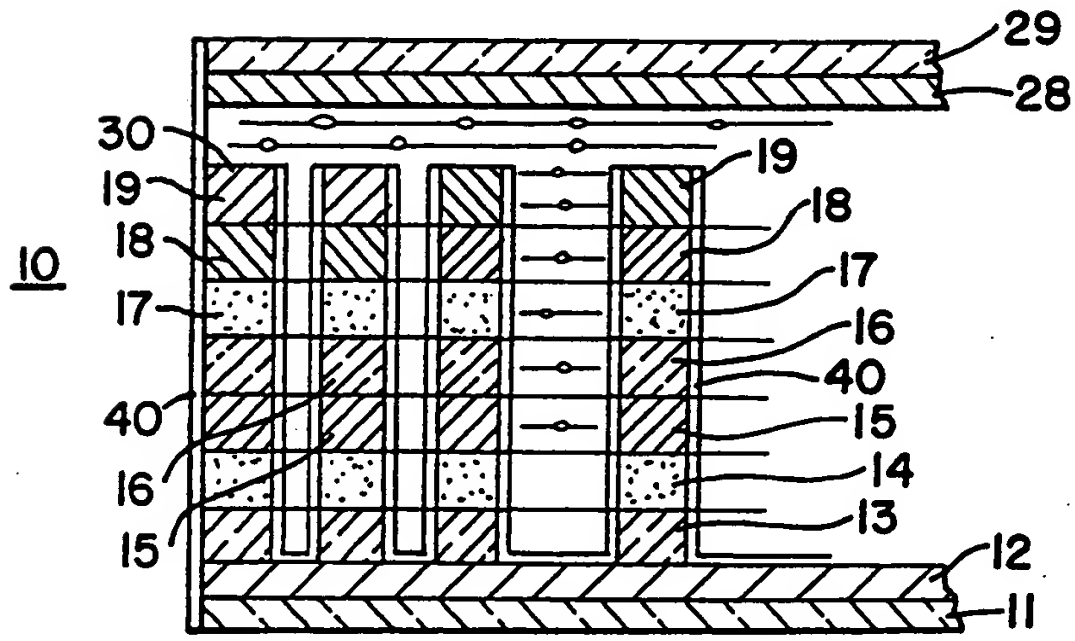
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FIG. 2

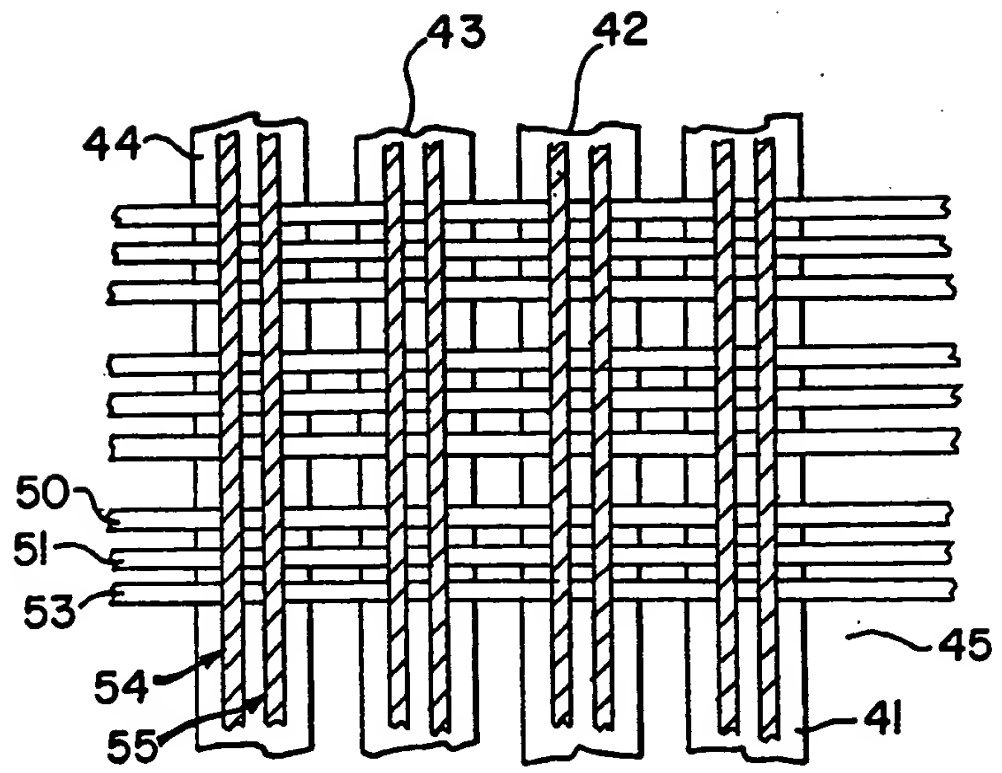
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FIG. 3

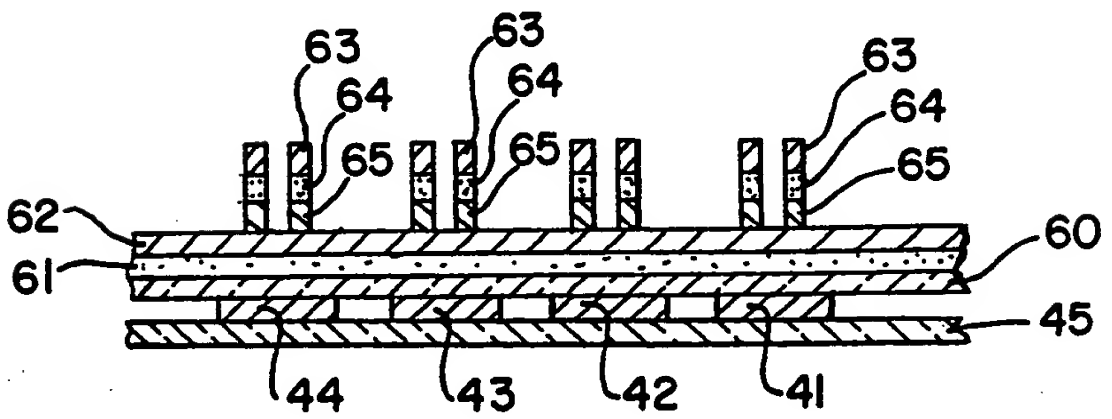
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FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/03759

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): C09K 19/00; G03C 5/00; G02F 1/13; B01D 61/42
U.S. CL. 430/20,394,312,314,316,318,319,329; 350/333,336,344, 339R; 204/299R; 428/1

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	430/20,312,314,316,318,319,329,394; 350/333,336, 344,339R; 204/299R; 428/1

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	US, A, 4,772,820 (DiSANTO) 20 SEPTEMBER 1988 See entire document.	1-20
A	US, A, 4,850,919 (DiSANTO) 25 JULY 1989 See entire document.	1-20
A	US, A, 4,732,830 (DiSANTO) 22 MARCH 1988 See entire document.	1-20
A	US, A, 4,680,103 (BEILIN SOLOMON I.) 14 JULY 1987 Claims 9-15.	1-20
A	US, A, 4,218,302 (DALISA) 19 AUGUST 1980 See entire document.	1-20
A	US, A, 4,655,897 (DiSANTO) 07 APRIL 1987 See entire document.	1-20
A	US, A, 4,522,472 (LIEBERT) 11 JUNE 1985 Claims 1-10.	1-20
A	US, A, 4,203,106 (DALISA) 13 MAY 1980 See entire document.	1-20
A	US, A, 3,668,106 (OTA) 06 JUNE 1972 Figures 1-12.	1-20

* Special categories of cited documents: [10]

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
30 JULY 1991	20 AUG 1991
International Searching Authority	**Signature of Authorized Officer**
ISA/US	Thomas R. Neville

Form PCT/ISA/210 (second sheet) (Rev.11-87)

(J.B. 08/07/91)

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(71) Applicant: COPYTELE, INC. [US/US]; 900 Walt Whitman Road, Huntington Station, NY 11746 (US).

(72) Inventors: DISANTO, Frank, J. ; 27 Par Court, North Hills, NY 11030 (US). KRUSOS, Denis, A. ; 1 Lloyd Harbor Road, Lloyd Harbor, NY 11743 (US). LASPINA, Christopher ; 58 Cherry Hill Lane, Syosset, NY 11791 (US).

(74) Agent: PLEVY, Arthur, L.; 146 Route 1 North, Edison, NJ 08817 (US).

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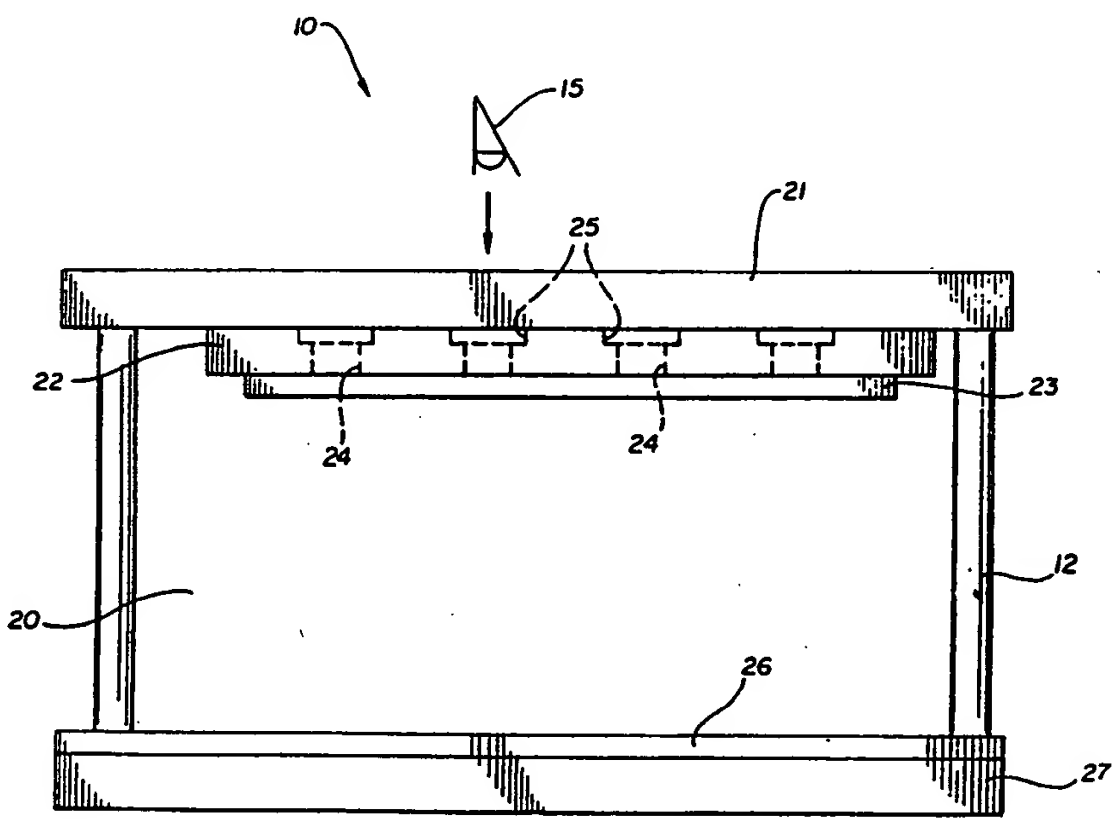
(54) Title: ELECTROPHORETIC DISPLAY EMPLOYING GREY SCALE CAPABILITY UTILIZING AREA MODULATION



(57) Abstract

An apparatus provides grey scale capability for an electrophoretic information display (10). The electrophoretic information display (10) is an XY addressable display with each XY coordinate indicative of a given column (23) and row (25) and defining a pixel. There are described means coupled to display for impressing upon the display a predetermined digital pattern to cause certain pixels in the display to be energized with respect to other pixels in the display where the combination due to the digital pattern causes a desired grey scale level to appear on a character or on the background of the display.

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Description

Electrophoretic Display Employing Grey Scale Capability Utilizing Area Modulation

Technical Field

The present invention relates to electrophoretic information displays (EPID) in general and more particularly to apparatus which operates in conjunction with an EPID display enabling such a display to operate with grey scale capability.

Background Art

The prior art is replete with a number of various patents and articles concerning electrophoretic displays. Such electrophoretic displays have been widely described and disclosed in the prior art and essentially the assignee herein, Copytele Inc., of Huntington Station, New York has developed an electrophoretic display which has an image area of approximately 11 x 8 1/2 inches and is designed to be used either as a separate display or to be combined with other displays. The company has the ability to combine as many as four such displays to create larger area displays. The information on such displays can be changed either locally or remotely and can be viewed at an angle of nearly 180 degrees. Such displays have been extremely high resolution and can accommodate over 160,000 pixels within an image area of approximately 2.8 inches diagonally.

In regard to such displays, reference is made to U.S. Patent No. 4,655,897 issued on April 7, 1987 entitled ELECTROPHORETIC DISPLAY PANELS AND ASSOCIATED METHODS to Frank J. DiSanto and Denis A. Krusos and assigned to Copytele Inc., the assignee herein. In

that patent, there is described an electrophoretic display panel which includes a planar transparent member having disposed on the surface a plurality of vertical conductive lines to form a grid of wires in the Y direction. On top of the grid of vertical lines, there is disposed a plurality of horizontal lines which are positioned above the vertical lines and insulated therefrom by a thin insulating layer at each of the intersection points. Spaced above the horizontal and vertical line pattern is a conductive plate. The space between the conductive plate and the X and Y line pattern is filed with an electrophoretic dispersion containing chargeable pigment particles. When a voltage is impressed on the X and Y lines, pigment particles which are located in the wells or depressions between the X and Y pattern are caused to migrate towards the conductive plate and deposited on the plate in accordance with the voltage applied to the X and Y conductors. There is described in that patent an electrophoretic dispersion suitable for operation with the display as well as techniques for fabricating the display. Hence, in this manner the displays can be fabricated to contain large effective display areas while being relatively thin. These displays are capable of high resolution and relatively low power consumption.

As indicated, the above noted patent and others include information concerning the fabrication, operation and resolution of such displays.

As explained in U.S. Patent No. 4,833,464, issued on May 23, 1989 and entitled ELECTROPHORETIC INFORMATION DISPLAY (EPID) APPARATUS EMPLOYING GREY SCALE CAPABILITY to Frank J. DiSanto, et al., it is a problem with such displays to provide grey scale

capability. Grey scale capability is a well known term of the art and has been utilized for example in regard to the description of television receivers and various other types of data presentation, such as facsimile and so on. In the case of television receivers, the response of the receiver can be visually determined by means of typical test patterns such as those test patterns that were previously transmitted and displayed when, for example, a television station goes off the air. Various television stations frequently transmit such a pattern for the convenience of service technicians and so on. The pattern apart from showing correct linearity, for example, also shows correct reproduction of the background shading which can indicate proper frequency response. The correct reproduction of the five color shades in the center target area of the test pattern indicates proper mid-frequency responses.

As one can ascertain, such test patterns are associated with grey scale capability, namely with the display of various grey levels as located between black and white. Such grey scale capability is a desirable feature in conjunction with any type of display. An electrophoretic display either presents a black or white type of representation of an image which is conveniently referred to as dark or light. Basically, the color of the image is a function of the color of the pigment particles and the color of the suspension that they are suspended in. The display may be black and white, yellow and black and so on.

There is a wide variety of many potential color combinations which can be employed in regard to such displays. The above-noted U.S. Patent No. 4,833,464, describes apparatus and techniques for grey scale

operation for an electrophoretic display panel. The apparatus includes circuitry which operates with a timing generator which produces a plurality of different time duration output wave forms which are applied to the X and Y drive as associated with the display. In this manner, by applying a set of voltages for a given duration time interval, a display is provided which results in the incomplete removal of pigment from associated selected pixels. Hence, those pixels appear darker than surrounding pixels but not as dark as the pure dye solution as associated with the display. Thus, the amount of pigment removed and hence the darkness of each pixel is a function of the time duration during which the appropriate voltage is applied to the rows and columns of the display. The timing generator can cause different pixels as displayed to have different darknesses or grey scale values by varying the time during which the voltage is applied to the display.

As will be further explained, grey scale operation at different shades of grey can also be provided on the electrophoretic display by means of area modulation. Area modulation can be used to shade either the foreground, the background or both the foreground and the background. Such electrophoretic displays, as other displays, portray information by writing in two different colors or shades of the same color. These, of course, can be referred to as black or white, although many other color combinations are available as indicated above. Thus, in an electrophoretic display, the normal background color is the color of the pigment used in the display and the written characters and graphics are generated by removing pigment from the appropriate areas. In the

reverse or inverse video mode the pigment is removed from the background while pigment is retained in the areas of the characters or graphics. This is the same difference, for example, between a negative and positive in photography. As will be explained, by performing area modulation by writing a pattern of either black or white pixels in either the background, foreground or both, permits generation of shades of grey. It is also understood that area modulation can be used with any relatively high resolution display to in fact provide a grey scale capability for the display.

It is therefore an object of the present invention to provide an electrophoretic display having grey scale capability.

It is a further object of the present invention to provide an electrophoretic display apparatus which has grey scale capability and which operates to modulate the area about each character or the area within each character on a display.

Disclosure of the Invention

Apparatus for providing grey scale capability for an electrophoretic information display (EPID), wherein said electrophoretic display is an X-Y addressable display with each X-Y coordinate indicative of a given column and row intersection, with each X-Y coordinate defining a pixel, which pixel when energized provides a different intensity display as compared to a non-energized pixel comprising of means coupled to said display for impressing upon said display a predetermined digital pattern to cause predetermined pixels in said display to be energized with respect to

other pixels in said display in accordance with a desired grey scale level.

Brief Description of the Drawings

Fig. 1 is a side plan view of an electrophoretic display (EPID) employed in this invention;

Fig. 2 is a perspective plan view of an electrophoretic display panel showing a given number of grid and cathode lines;

Fig. 3 is a graph depicting a character block displayed on a conventional black and white display;

Fig. 4 depicts a character displayed with a predetermined area modulated background pattern;

Fig. 5 shows still another area modulated pattern;

Fig. 6 is a diagram showing still another pattern;

Fig. 7 is a diagram showing still another pattern;

Fig. 8 is a diagram showing an alternate pattern;

Fig. 9 is a diagram showing still another alternate pattern;

Fig. 10 is a diagram of a character block showing an alternate background pattern;

Fig. 11 is a diagram of a character block showing an alternate background pattern;

Fig. 12 is a schematic diagram partially in block form showing a circuit for deriving a grey scale value for an electrophoretic display employing area modulation;

Fig. 13 shows an OR gate employed in this invention;

Fig. 14 shows an AND gate employed in this invention;

Fig. 15 shows a logic circuit for providing grey background or characters; and

Fig. 16 shows a logic circuit for providing the character and background features.

Best Mode for Carrying Out The Invention

Referring to Figure 1, there is shown a side view of a typical electrophoretic display 10. The display 10 of Figure 1 is filled with an electrophoretic solution 20 which includes light colored pigment particles suspended in a dark dye solution. For examples of such solutions and techniques, reference is made to the above cited U.S. Patent No. 4,655,897.

It is also understood that the display can consist of a dark pigment suspended in a light solution and so on. As seen from Figure 1, the display contains a front glass sheet or viewing surface 21. The eye of the viewer 15 is shown viewing the front of the display via the glass sheet 21. Superimposed upon the glass sheet 21 by suitable etching techniques are columns 23 and rows 25. The rows are made from an extremely thin layer of idium-tin-oxide (ITO) while the columns are made from thin layers of aluminum or other suitable metal. These patterns, as indicated, are provided in extremely thin layers and constitute an XY matrix. The layers of ITO as can be seen by reference to the above-noted patent are relatively thin being approximately 3000 Angstroms thick. The grid or columns and the rows or cathodes (XY) are spaced from one another and insulated from one another by means of an insulating layer 22. While the grids and cathodes have been specified in terms of rows and columns, it is understood that the terms can be interchanged as desired. Each of the grid and

cathode intersections are associated with a pigment well 24. These wells contain electrophoretic solution which is in the cavity 20. The columns and rows are separated from a back electrode 26 which is also fabricated on a sheet of glass 27 and constitutes a thin layer of ITO. The spacers such as 12 and 23 can be implemented in many different ways and essentially serve to mechanically separate the display or panel 10. In operation of the display, the pigment particles contained in the electrophoretic solution 20 are brought forward towards the viewing surface in order to fill the wells formed between the rows and columns. Once a well such as 24 is filled, the voltage on the tows and columns and rear cover is then set, such that the wells remain filled, but pigment spaced between the rear cover and the columns are swept onto the rear cover plate 26. At viewing side 21, one sees the color of the pigment in the wells. By selectively applying voltages to the rows and columns, the pigment in the individual wells 24 (at the intersection of the rows and columns selected) is forced out of the wells exposing the dye solution and making that intersection (pixel) dark. The removal of the pigment from the wells is not instantaneous but requires a period of time which depends upon the dimension of the cell or display, the fluid components, and the various supply voltages. The above-noted U.S. Patent No. 4,833,464 discusses the control of the voltages and the duration of the same to control grey scale operation. The techniques for performing area modulation in conjunction with an electrophoretic display will be described in detail.

Referring to Figure 2, there is shown a plan view of an enlarged representation of an electrophoretic

display cell or panel according to Figure 1. As seen in Figure 2, each well is accommodated between an intersection of a column metal layer 23, which is insulatively separated from a row layer of ITO 25. The well 24 forms a pixel area which is indicative of an XY intersection of the ITO display. Thus, as one will understand, the object of the present invention is to provide grey scale capability and this grey scale capability is performed in a high resolution electrophoretic display. It is noted that the resolution of the display has to be high to accommodate area modulation and derive the particular aspects and benefits of this technique.

Referring to Figure 3, there is shown a representation of the letter E as for example, displayed on a conventional electrophoretic display. In regard to the following discussion, it will be indicated that the states of the electrophoretic display, for example as shown in Figure 3, are black and white. It is understood that the letter E will be visible if the pixels were darker than the background.

As indicated above, area modulation is accomplished by writing a pattern of either black or white pels in either the background, the foreground or both. The high resolution provided by an electrophoretic display permits the use of area modulation to generate shades of grey. Area modulation can be employed with any relatively high resolution display. Appearance of the grey scale due to area modulation is a physiological consequence of the resolution of the human eye. The effect is obtained when the angle suspended by the black and white pels as seen by the viewer, approaches the resolution of the human eye. In a typical

electrophoretic display as provided by the assignee herein, Copytele Inc., a resolution of 200 lines per inch in both the horizontal and vertical directions is available.

This resolution is ideal for producing grey scale by means of area modulation. On an electrophoretic display with this resolution, characters are written using a character block of 16 pixels horizontally and 24 pixels vertically. As seen in Figure 3, both the horizontal and vertical directions are indicated by means of gradations as 30 and 31. These gradations encompass an area which is indicative of a pixel. Hence, as one can see, there are essentially 16 boxes or pixels representing the top line in the image area 32 depicted in Figure 3. Thus, again referring to Figure 3, it is indicated that with the above-noted resolution of 200 lines per inch in both the horizontal and vertical directions, character blocks consisting of 16 pixels or pels horizontally and 24 pels vertically are typical. This character block yields a display with 25 lines of 80 characters each on a display whose dimensions are approximately 6.4 x 3.2 inches. Thus, as one can ascertain from Figure 3, there is shown the character E which is represented in black on a relatively white background. It is, of course, understood that the inverse of this image could also be provided by the electrophoretic display.

Referring to Figure 4, there is again shown the character E within the character block 32 having a 50 percent grey background. Essentially, the character E is the same as shown in Figure 3 but the background consists of alternate pixels of black and white as can be seen, for example, from Figure 4. Across the top line 40, the 16 pixels are indicative of white, black,

white, black and so on. On line 41, the pattern is black, white, black, white and so on. This pattern then continues to alternate down and across the display so that it alternates as to the 16 horizontal pixels and the 24 vertical pixels. The background appears grey when the image is viewed at a distance where the individual pels are unresolved. Because of this property, the number of grey shades obtainable via area modulation is again a function of the display's resolution, the size of the character and the viewing distance. As one can ascertain, the background area is modulated accordingly to produce patterns which have grey scale capability due to the nature of the modulation technique.

Referring to Figure 5, there is shown the character block which now possesses an area modulated background which is 93.25 percent black. This is obtained by formulating each horizontal line within the character block, all within the display area by means of a particular Hex code. As seen in Figure 5, line 50 is indicative of the Hex code EE where black is equal to binary one and white is equal to binary 0. Based on the display format shown in Figure 5, in order to obtain a background which his 93.25 percent black, one modulates the display lines as follows. The first line 50 as seen is BBBWBBBWBBBWBBBW (Hex EE). The next three lines 51, 52, and 53 are all black or all B (Hex FF). The fourth line is BWBBBWBBBWBBBWBB (Hex BB). At the right of each line, there is shown the Hex code for the line. As one can see from the Hex code notation, it is a repetitive pattern which specifies the display background as in Figure 5 to obtain a background which is 93.25 percent black. The line pattern for the display of Figure 5

is HEX, EE, FF, FF, FF, BB, FF, FF, FF and repeats for the 24 lines.

Referring to Figure 6, there is shown an area modulated background or character block which is 87.5 percent black. The Hex line values are shown at the right hand side to denote the repetitive pattern. As one can see from Figure 6, line 61 is BWBBBWBBBWBBBWBB which is Hex code BB. Line 62 is all black which is Hex FF. Line 63 is BBBWBBBWBBBWBBBW which is hex code EE. Line 64 is all black as Hex code FF.

Referring to Figure 7, there is shown an area modulated background pattern which is 62.5 percent black. The Hex code is shown at the right and is a relatively simple repeating code with the first line 70 being WBBBWBBBWBBBWBBB or Hex 77. Line 71 is BBWBBBWBBBWBBBWB which is Hex DD and then the pattern repeats as Hex 77, DD, 77, DD, 77, DD...etc.

Referring to Figure 8, there is shown a pattern which is 50 percent black and has a simple repeat as line 80 is BWBWBWBW... etc. Line 81 is WBWBWB etc. which respectively denotes the Hex code of AA and 55, which code repeats for the 24 lines.

Referring to Figure 9, there is shown an area modulated display or character block which is 37.5 percent black. The Hex code is shown on the right as line 90 is Hex code AA as for example indicative of line 80 of Figure 8, while line 91 is Hex code 44 which is WBWWWBWWWBWWWBWW. Line 92 is the same as line 90 (AA) while line 93 is Hex code 11 or WWWBWWWBWWWBWWWB. The code then alternates as seen in Figure 9.

Referring to Figure 10, it depicts a character block or display having 25 percent black background.

The Hex code is shown on the right hand side for each line.

Referring to Figure 11, it shows a display or character block, the Hex code again at the right exhibiting a 12.4 percent black background. As one can ascertain, the above-noted figures essentially depict six different patterns which six patterns will yield seven different shades of grey when viewed at normal viewing distance on a 200 x 200 line per inch electrophoretic display. These patterns coupled with black and white yield a system with nine shades of grey. However, in practice, a background of 12.5 percent black can be omitted as exhibiting a small difference from white. The patterns as one can easily ascertain, which are distinct are shown in Figures 5-11. These figures represent various patterns which yield different shades of grey when viewed at a normal viewing distance on a 200 x 200 line per inch electrophoretic display.

The system as shown with a 200 line resolution including black and white can produce eight different effective shades of grey. The patterns used to achieve area modulation in a character type or graphics type display when the graphics are formed using special characters must be a factor of the character block. For example, in a display using a character block which is 16 pixels wide and 24 pixels high, the width of the area modulated pattern must be a factor (divisor) of 24 and the height of the pattern must be a factor (divisor) of 16. The figures shown in the above-noted application, as indicated for example in Figure 3, are patterns which are designed for a 16 x 24 pel character block. The figures show patterns which have increasingly more white (less

grey), however, the actual grey shade that the human eye perceives is dependent upon many factors including display type, ambient lighting, color and other factors. It may be necessary to have unequal increments in the percentages of black and white in successive patterns to generate scales which are subjectively more and more grey.

There are many techniques as one can imagine for accommodating area modulation which can be implemented simply by using registers and appropriate gating modules.

Displays using shades of grey require that an attribute which describes the image foreground and background colors be designed for each character. The attribute length depends on the total number of different color combinations required. For example, if only one intermediate shade of grey is required between black and white then there are only six combinations of foreground/background colors. These six states are most readily encoded using 4 bits. Bit 0 and 1 specify the foreground color while bits 2 and 3 define the background color. In typical display systems, a byte is devoted to the attribute even though not all 64 states definable by 8 bits are used. The implementation of such a system can be done in a variety of ways.

Simple implementation for generating a grey background is to OR the pel data and the selected AM pattern (Black = binary 1 and White = binary 0). This can be done in real time as the pel data and the character data is loaded into shift registers or into the drive circuitry. In systems which use a pixel memory it can be done as the pel data is generated or is loaded into the pixel memory. To make the

characters or graphics a shade of grey, the procedures described can be used except that the "OR" function is replaced with an "AND" function. In inverse video, the function used to obtain a grey background is the AND function between the pixel data and the amplitude modulated pattern. To make the characters grey in inverse video, one would employ the OR function.

Referring to Figure 12, there is shown a circuit configuration in block form for an electrophoretic display panel 10 which is associated with area modulation as described above. Of course, it is understood that the cathodes and grids while described previously in the XY planes can be reversed whereby the cathode lines can be arranged in the Y plane with the grid lines in the X plane or vice versa. As one can see from Figure 12, each Y line such as 30 and 31 is associated with suitable drive amplifiers 32 and 33, where each X line such as lines 34 and 35 are associated with suitable amplifiers 36 and 37. It is of course seen in Figure 12, that the dots or dashes between amplifiers 36 and 37 and 32 and 33 are employed to indicate a plurality of additional individual amplifiers indicative of a large number of lines. In this manner, by applying proper biasing potentials to respective amplifiers, one can cause pigment particles to migrate at any intersection between the X and Y matrix as formed by the associated grid and cathode lines. Thus, based on the X and Y matrix, one can therefore produce any alphanumeric character. For such displays with a large plurality of intersections or pixels, one can provide graphic data such as a television picture and types of other displays on the display panel 10. The display which is the electrophoretic display is provided with high

resolution based on the technique of fabricating line patterns and based on presently available display techniques. The driver amplifiers 32 and 33 and 36 and 37 are fabricated by typical integrated circuit techniques and may for example by CMOS devices, which are well known and many of which are available as conventional integrated circuits. As indicated, the resolution of the electrophoretic display panel is high based on modern integrated circuit techniques and including the fabrication techniques employed in conjunction with such displays. It is anticipated that the resolution of such displays can be as high as 40,000 dots per square inch. As seen from Figure 12, the Y amplifier such as 32 and 33 are coupled to a Y address register 41. The address register 41 is a well known component consisting of various conventional decoding devices including buffer registers and so on for the storage of data and interfacing with the various columns associated with display 10. In a similar manner the amplifiers 36 and 37 have inputs coupled to an address module 40 which is similar to module 41 and operates to provide the Hex address information for the XY intersections provided by the display. Means for addressing an XY matrix is solved by many typical circuit solutions in the prior art and such decoders as the Y address register 41 and the X address register 40 are well known components in the prior art.

Both the X and the Y address registers are coupled to master decode module 50 which operates to decode data and to generate the X and Y addresses for such data as is conventionally known.

Coupled to the decode module 50 which again may be a typical microprocessor or another programmed

device is an area modulation memory 51. The area modulation memory 51 contains in storage suitable digital patterns, such as for example the Hex codes as shown in Figure 4-11 which will enable one to produce a display according to a desired grey background. The stored data as indicated is associated with 4 bits which determine the darkness or content of both the background and foreground depending upon whether one wants to introduce the grey in the foreground or to introduce the grey in the background. The area modulation memory contains the patterns as shown in the above-noted figures to enable one to provide 6 or more levels of grey associated with a particular display and according to the preference of the user. It is, of course, indicated that each line of the display can be modulated by means of the code contained in memory 51 to thereby produce a uniform grey or other background for the entire display. In a similar manner, one can also modulate each character block in a different manner or modulate each line in a different manner or a portion of the display to produce various grey formats throughout the display. This can enable one to highlight certain regions of the display or certain areas of the displayed text with respect to the other areas and according to the intensity of the foreground or background. The decode module 50 is also coupled to a character generator 52 which character generator is a conventional component. The character generator 52 is coupled to a keyboard 53. The character generator 52, the decoder 50 and the keyboard 53 may be part of a conventional computer system such as a PC system. There is another path shown in Figure 12, whereby there is a data receiver 57 which is capable of receiving data from a typical

telephone line or other transmission medium. This data receiver may be a conventional modem. The output of the data receiver is coupled to an analog to digital converter 56 for transforming the analog signals at the input to digital signals at the output of the analog-to-digital converter 56. The analog-to-digital converter 56 is associated with a digital signal pixel generator 58 which operates in conjunction with the master decoder 50 to allow one to perform area modulation at various pixel sites as desired. The output of the decoder 50 is also coupled to the X address register and the Y address register 40 and 41. The area modulation memory 51 is shown coupled to the decoder 50, but can of course be part of the microprocessor memory where a certain section will be reserved for the different area modulation background codes. As shown in Figure 12, the module designated as grey scale select 60 is coupled to the area modulation memory 51. The module 60 decodes the particular grey scale request which data may be forwarded to the module 60 by means of the character generator 52 or by means of the decoder 50. In this manner, the system by decoding the transmitted data would automatically determine what grey scale is to be utilized for a particular display. This can be automatically done by means of suitable decoders or can be implemented at the preference of the user. As shown in Figure 12, the character generator 52 is also coupled to the grey scale select module 60 and a user while viewing an image can go ahead and select the grey scale value desired and according to the preference of the user. As one can immediately ascertain from Figure 12, area modulation can be simply implemented. One technique of implementing the

area modulation is that the decoder or microprocessor 50 combines the area modulation code as stored in the area modulation memory with the data code. For example, if black is equal to 1 and white is equal to 0 then an "AND" or "OR" function can be used. In the OR function, whenever a pixel does not contain data, the pixel would receive the exact binary digit indicative of the background code. Where a pixel does contain data, the output will be a 1 if the data is a 1. If the data is 0 and the background is a 1, the output would also be a 1 according to the area modulation pattern as stored. Thus, the OR function provides a full black or dark character with the selected grey background as stored in the area modulation memory 51. Thus, the patterns depicted in the above-noted Figures 5-11 can be combined with he data pattern, to provide AND and OR functions or both as will be further explained. To present the characters or graphics with a desired shade of grey, the procedures described above can be used except the OR is replaced with an AND function.

In this manner, both the data and the area modulation bit must be the same in order to produce a black spot at the output. If they are not the same then the color of the pixel remains white. As one can see, one will produce a character having a different grey scale which is presented on an all white or in the case of a negative application on an all black background. In an inverse video mode the function used to obtain a grey background is the AND function occurring between the pixel data and the stored area modulation pattern. To make the characters grey in an inverse video mode, one would employ the OR function between a grey background pattern and a pixel data

pattern. As indicated above and briefly described, either the characters (foreground) or the background of a display can have grey scale. Both these options and the no grey scale option can be readily generated by means of simple combinatorial circuits.

Referring to Figure 13, no grey scale requires no gating. The grey background is accomplished by OR gating the character data bit stream with the grey scale pattern bit stream as shown in Figure 13. Thus, as indicated in Figure 13, there is shown an OR gate 70 with one input designated as CHAR representative of the character bit stream and the other input designated as the grey bit steam.

As one can ascertain, the grey bit stream would be that stream or data which has been defined in conjunction with Figures 5-11.

Referring to Figure 14, there is shown an AND gate 71 having one input designated as by CHAR and indicative of the character bit stream and the other input receiving the grey bit stream as again shown in the above-noted figures. The output of the AND gate 71 is directed to the display or to the display drivers as is the output of gate 70. The grey characters are generated by the AND gate 71 which will produce grey character on a constant background. Typically, the color of each character can be described by a number of additional bits which are designated as attribute bits or an attribute byte. This set of bits or byte are normally required for each character to be displayed. The number of bytes of attribute data could be reduced by means of many different schemes which are not pertinent to this aspect of the invention. For example, an attribute

byte with the following bit interpretations can be employed for generating grey scale displays.

00000000 no grey scale (black characters on white.

00000001 grey background with black characters.

00000010 grey characters with white background.

It is noted that in the above examples only 2 bits, as for example, the first and second bits are needed to generated the grey display. The other bits typically are used to specify the shade of grey desired. For simplicity, assume the desired grey shade has been selected and will be used when grey is required. With these assumptions and the example attribute code specified above, only a simple logic circuit is required to generate the required bit stream.

Referring to Figure 15, there is shown a logic circuit capable of generating an output signal for the display which provides a grey background or a grey character as controlled by the attribute bits. As seen in Figure 15, the attribute bits designated as A0 and A1 define the type of display. For example, 00 is no grey, 01 is a grey background and 10 is a grey character. As one can see, the character bit stream is directed to a 3 input AND gate 80 and is also directed to a 2 input AND gate 81. The grey bit stream is directed to one input of an OR gate 82 and to one input of the AND gate 81.

In this manner, as one can ascertain, the attribute bits which are A0 and A1 are applied to inverters 83 and 84. The output of inverter 83 is directed to one input of AND gate 80 and one input of AND gate 85. The output of inverter 84 is applied to one input of AND gate 80 and to one input of AND gate

86. The output of OR gate 82 is coupled to one input of AND gate 86 while the output of AND gate 81 is coupled to input of AND gate 85. As seen, the AND gates 85 and 86 also receive the attribute bits which are the uninverted bits. The outputs of the three AND gates 85, 86 and 80 are coupled to three inputs of an output OR gate 87, which supplies the output display bit stream. For the combination of attribute bits, the bit streams are suitably directed through appropriate gates to provide a grey background with a black character, to provide no grey, or to provide a grey character on a light background. The logic implemented by the circuit should be well understood by those skilled in the art.

Referring to Figure 16, there is shown a logic arrangement which based on the attribute bit table shown will produce either no grey, a grey background, a grey character, grey background of a given intensity or a grey background of another intensity specified as grey No. 2. Thus, as seen in the Figure 16, the attribute bits A1 and A0 can combine to produce no grey, a grey 1 background with black characters, grey No. 2 with a white background, grey No. 1 background with grey No. 2 characters. Thus, the logic circuit shown in Figure 16 defines a simplified logic circuit which is predicated on using either a grey pattern of a first intensity for the background and another grey pattern of a different intensity for the foreground and so on. These are indicated as a grey No. 1 pattern and a grey No. 2 pattern. Both of these patterns are typical of those patters, for example, shown in Figures 5-11 as described above. Again the character bit stream is inserted into the circuit with

the attribute bits A0 and A1 having the binary characteristics depicted in the table of Figure 16.

In a similar manner, the circuit of Figure 16 has four output AND gates designated as 90, 91, 92 and 93 with gate 90 being a no grey gate, gate 91 producing the grey 1 output as a background, gate 92 producing the grey 2 character and gate 93 enabling one to provide a grey 1 background and a grey 2 character. A description of each of the individual gates in the uninverted state as for example, gate 93 receives the A1 uninverted as does gate 92, while gates 91 and 90 receive the A1 inverted signal. One can immediately ascertain the operation of the above-described circuit by referring to Figure 16.

Claims

1. Apparatus for providing grey scale capability for an electrophoretic information display (EPID), wherein said electrophoretic display is an X-Y addressable display with each X-Y coordinate indicative of a given column and row intersection, with each X-Y coordinate defining a pixel, which pixel when energized provides a different intensity display as compared to a non-energized pixel comprising:

means coupled to said display for impressing upon said display a predetermined digital pattern to cause predetermined pixels in said display to be energized with respect to other pixels in said display in accordance with a desired grey scale level.

2. The apparatus according to Claim 1, wherein said pixel when energized causes a dark intensity to be displayed as compared to a lighter intensity when not energized with said darker intensity corresponding to a black level and with said lighter intensity corresponding to a white level.

3. The apparatus according to Claim 1, wherein said digital pattern is impressed on said display by means of AND logic means to cause characters as written on said display to exhibit said grey scale level with respect to the background of said display.

4. The apparatus according to Claim 1, wherein said digital pattern is impressed on said display by means of OR logic means to cause said background to exhibit said grey scale level with respect to characters on said display.